20-bit Sigma Delta ADC

The SDADC20 is a 20-bit analog to digital converter implemented as a Sigma Delta architecture. The ADC has programmable analog and digital gain settings. Analog gains of 1x or 2x are selected by an analog gain stage before the data converter. Digital gains of 1x, 2x, 4x, 8x, 16x, 32x, 64x and 128x are selected after the digital decimation filter. The ADC supports offset and gain calibration. The calibration routing calibrates the input voltage standard to a digital full scale output code. The offset and gain calibration results are stored in on chip registers. The offset and gain calibration results can be overwritten during normal operation. Programmability of the ADC's decimation filter, digital gain and analog gain allow for tuning of the converter's data rate, noise and resolution for different modes of operation. The ADC can operate in single-end or differential mode. The digital output formats for single-ended and differential modes are shown in the tables below.

Single-ended Operation ADC Output Format

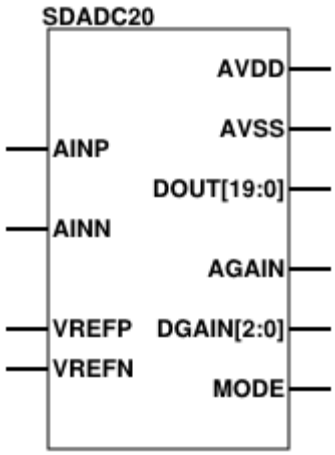
Single-ended Input Voltage	Output Code (Offset binary format)
+full scale	FFFFFh
zero	00000h

Differential Operation ADC Output Format

Differential Input Voltage	Output Code (Offset binary)	Output Code (two's complement)
+full scale	FFFFFh	7FFFFh
zero	80000h	00000h
-full scale	00000h	80000h

SDADC20 Symbol and Pinout Table

Pin Name	Type	Function	
AINP	Analog Input	Positive analog input	
AINN	Analog Input	Negative analog input	
VREFP	Analog Input	Positive analog reference voltage	

VREFN	Analog Input	Negative analog reference voltage	
MODE	Digital Input	Single-ended or differential input mode	
DGAIN[2:0]	Digital Input	Digital Gain Select	
AGAIN	Digital Input	Analog Gain Select	
DOUT[19:0]	Digital Output	ADC Digital Data	
AVSS	Analog Power	Ground reference	
AVDD	Analog Power	Analog power	

Performance Characteristics

Parameter	Description	Notes/Conditions	min	typ	max	units
ADC_{VHIGH}	Input voltage upper limit				VDD-100mV	V
ADC_{VLOW}	Input voltage lower limit		AVSS+100mV			V
ADC_{VRANGE}	Input dynamic range	Single-ended Differential (ADC_{VHIGH} - ADC_{VLOW})	0 $-V_{REF}$		V_{REF} $+V_{REF}$	V
	Common Mode Voltage Range		AVSS+100mV	VDD/2	VDD-100mV	V
ADC_{RES}	Resolution	**60Hz Notch Mode** Resolution @ 10 sps Resolution @ 20 sps Resolution @ 40 sps Resolution @ 80 sps Resolution @ 160 sps Resolution @ 320 sps Resolution @ 640 sps **50Hz Notch Mode** Resolution @ 8.333 sps Resolution @ 16.667 sps Resolution @ 33.333 sps Resolution @ 66.667 sps Resolution @ 133.333 sps Resolution @ 266.667 sps Resolution @ 533.333 sps		 20.0 19.0 19.0 18.0 16.0 13.0 11.0 20.0 19.0 19.0 18.0 16.0 13.0 11.0		bits
ADC_{DNL}	Differential nonlinearity				±1	LSB

ADC_{INL}	Integral nonlinearity	Uncalibrated			±11	LSB
	Zero Error after calibration	ppm of full scale reference	-10		+10	ppm FSR
	Zero Drift	zero code drift vs temp		50		nV/℃
	Full Scale Error after calibration	ppm of full scale reference	-20		+20	ppm FSR
	Full Scale Error Drift	full scale code drift vs temp		0.05		ppm FSR/℃
ADC_{PSSR}	Power Supply Rejection			TBD		dB
ADC_{CMR}	Common Mode Rejection			TBD		dB
	Normal Mode 50/60Hz Rejection		100			dB
G	Input Voltage Gain	Programmable	1		128	
	Data Rate	Programmable	2.5	10	400	SPS
V_{REF}	Reference Voltage		1.8	2.5	3.2	V
V_{CMO_IN}	Input Common Mode Voltage		100	2.5	4	mV

SDADC20 Simplified Internal Circuit Schematic